the control electrodes of said first and second transistors are supplied with a differential input signal; and

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

3. (Amended) The differential amplifier circuit as claimed in claim 1, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

4. (Amended) The differential amplifier circuit as claimed in claim 1, wherein the differential input portion further comprises:

a fourth transistor for supplying a drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; wherein

said third transistor is connected in parallel to said fourth transistor.

5. (Amended) The differential amplifier circuit as claimed in claim 4, wherein the control electrode of said third transistor is supplied with a first control signal for constantly supplying the minute current during the operation of said differential amplifier.

8. (Amended) The differential amplifier circuit as claimed in claim 1, wherein a first control signal supplied to the control electrode of said third transistor is

set to a level for supplying a predetermined drive current at the time of signal determination in said differential amplifier circuit, while causing the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

11. (Amended) The differential amplifier circuit as claimed in claim 1, further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

15. (Amended) The differential amplifier circuit as claimed in claim 1, further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

17. (Amended) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal; and

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

22. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

23. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein the differential input portion further comprises:

a fourth transistor for supplying a drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; wherein

said third transistor is connected in parallel to said fourth transistor.

27. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein a first control signal supplied to the control electrode of said third transistor is set to a level for supplying a predetermined drive current at the time of signal determination in said differential amplifier circuit, while causing the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

30. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

34. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

A marked-up copy of the amended claims is attached as required under 37 C.F.R. § 1.121.

Please add new claims 36-39 as follows:

36. (New) A receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting a differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path, the receiving circuit comprising:

a differential amplifier circuit receiving the differential signal, said differential amplifier circuit including a latch unit and a differential input portion, wherein a minute current is kept to flow through said differential input portion;

a latch circuit latching an output signal of said differential amplifier circuit;

a clock source generating a clock and supplying the generated clock to said differential amplifier circuit; and

an equalizer circuit, receiving the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

37. (New) The receiving circuit of a signal transmission system as claimed in claim 36, comprising a plurality of receiving units each including said differential amplifier circuit, said latch circuit and said equalizer circuit, said plurality of receiving units carrying out an interleave operation.

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38. (New) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receiving a control signal; and

an eighth transistor inserted between said second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.